Include waveLogicUnit.do and waveArithUnit.do! I’ve made changes

Changed TimingArithUnit.do to run for 15600 ns.

**Notes**:

* We don’t document the testbenches for part 1
* DO NOT add listings of your source code to the report.
* **The final project documentation (single zip file called “FP1-Gxx-350-1201.zip”) are**
  + Final project report (THIS FILE)
  + VHDL source code for all (three) design entities.
  + 4 transcript files,
  + A summary file (called “FP1-Summary-Gxx-350-1201.txt”) – created by merging these four summary files.
    - LogicUnit.map.summary
    - ArithUnit.map.summary
    - LogicUnit.fit.summary
    - ArithUnit.fit.summary,
    - Insert title lines to ensure that the individual summary reports are easily distinguishable.
  + The two post-fit netlists (LogicUnit.vho, ArithUnit.vho)
    - Each screen clipping from a netlist viewer should occupy a full page
    - Each image should have a title and brief description
    - The image should contain both the zoomed view and the window for birds eye view
  + The two standard delay format files (LocicUnit.sdo, ArithUnit.sdo)
  + WaveLogicUnit.do and/or WaveArithUnit.do. (only if you modified them)

**Design Entities**

64-bit ripple carry adder

Functional Behaviour

The arithmetic unit uses a 64-bit ripple carry adder to perform addition. It is built from chaining 64 1-bit full adders, which each have three inputs and two outputs . The relationship is The and status signals are set such that two 1’s produce a Y of 0 and of 1. If two 1’s are added, and the is also 1, then both Y and are also 1. The overflow status signal is set when either two positive numbers are added and a negative number is returned, or when two negative numbers are added, and a positive number is returned.

VHDL Interface

A screenshot of a cell phone

Description automatically generated

Circuit Diagram

The overflow hardware can be implemented by realizing that if either the last carry-out bit or the next-to-last carry-out bit are 1, then overflow has occurred. Therefore, if the XOR of the last and next-to-last carry-outs is 1 then there has been overflow

A close up of a logo

Description automatically generated

64-bit Arithmetic Unit

Logic Unit

Simulation Runs

* Include these produced transcript files in the final zip submission
  + FuncLogicUnitTranscript.txt
  + FuncArithUnitTranscript.txt,
  + TimeLogicUnitTranscript.txt
  + TimeArithUnitTranscript.txt,

Simulation Waves

* The simulation waveforms all need titles and annotations.
* Two images per landscape page
* Discussion that explains why this simulation run verifies the functional behaviour and timing of the tested entity.