Include waveLogicUnit.do and waveArithUnit.do! I’ve made changes

Changed TimingArithUnit.do to run for 15600 ns.

**Notes**:

* We don’t document the testbenches for part 1
* DO NOT add listings of your source code to the report.
* **The final project documentation (single zip file called “FP1-Gxx-350-1201.zip”) are**
  + Final project report (THIS FILE)
  + VHDL source code for all (three) design entities.
  + 4 transcript files,
  + A summary file (called “FP1-Summary-Gxx-350-1201.txt”) – created by merging these four summary files.
    - LogicUnit.map.summary
    - ArithUnit.map.summary
    - LogicUnit.fit.summary
    - ArithUnit.fit.summary,
    - Insert title lines to ensure that the individual summary reports are easily distinguishable.
  + The two post-fit netlists (LogicUnit.vho, ArithUnit.vho)
    - Each screen clipping from a netlist viewer should occupy a full page
    - Each image should have a title and brief description
    - The image should contain both the zoomed view and the window for birds eye view
  + The two standard delay format files (LocicUnit.sdo, ArithUnit.sdo)
  + WaveLogicUnit.do and/or WaveArithUnit.do. (only if you modified them)

**Section headers so far:**

Design Entities

* For each Design Entity
  + A paragraph describing the functional behaviour of the entity.
  + The VHDL entity declarations (ArithUnit, LogicUnit, Adder)
    - reference the name of the VHDL source file which is attached
  + A circuit diagram for the entity.
    - all labels must identically match your VHDL source code.

Simulation Runs

* Include these produced transcript files in the final zip submission
  + FuncLogicUnitTranscript.txt
  + FuncArithUnitTranscript.txt,
  + TimeLogicUnitTranscript.txt
  + TimeArithUnitTranscript.txt,

Simulation Waves

* The simulation waveforms all need titles and annotations.
* Two images per landscape page
* Discussion that explains why this simulation run verifies the functional behaviour and timing of the tested entity.